LISTING OF THE CLAIMS

Claim 1 (Withdrawn) A method of forming a plurality of conductive structures on a substrate comprising the steps of:

forming a first semiconductor structure of a first conductivity type, a second semiconductor structure of a second conductivity type, and a third semiconductor structure on a substrate, said third semiconductor structure is disposed between said first and second semiconductor structures and is separated therefrom by an insulator structure;

depositing an interconnect layer over at least said first, second and third semiconductor structures;

forming a planarizing conductor on said interconnect layer, said planarizing conductor having etch characteristics similar to those of said interconnect layer and said first and second semiconductor structures, but different from those of said insulator structure; and

patterning and etching said planarizing conductor, said interconnect layer, and said first and second semiconductor structures so that each has at least one lateral dimension that is substantially the same.

Claim 2 (Withdrawn) The method of Claim 1 wherein said first and second semiconductor structures are formed utilizing a double angled implant such that vertical surfaces of a polySi-containing or semiconducting layer formed abutting said insulator structure are oppositely doped, while horizontal surfaces of said polySi-containing or semiconducting layer are doubly doped.

Claim 3 (Withdrawn) The method of Claim 2 wherein said polySi-containing layer is comprised of polySi.

Claim 4 (Withdrawn) The method of Claim 2 wherein said polySi-containing layer is comprised of polySiGe.

Claim 5 (Withdrawn) The method of Claim 2 wherein said double angled implant is performed so as to provide implant regions whose final dopant concentration is on the order of from about 1E19 to about 1E21 atoms/cm^3.

Claim 6 (Withdrawn) The method of Claim 1 wherein said insulator structure includes a gate dielectric and a hard mask.

Claim 7 (Withdrawn) The method of Claim 1 wherein said interconnect layer is a metallic layer which is capable of preventing dopant diffusion into said first and second semiconductor structures.

Claim 8 (Withdrawn) The method of Claim 1 wherein said planarizing conductor is comprised of a polySi-containing material, a conductive metal, a conductive metal alloy or a semiconducting material.

Claim 9 (Withdrawn) The method of Claim 8 wherein said planarizing conductor is comprised of polySi or polySiGe.

Claim 10 (Withdrawn) The method of Claim 1 further comprising annealing said interconnect layer so as to convert said layer into a metal silicide or metal nitride.

Claim 11 (Withdrawn) The method of Claim 10 wherein said annealing is carried out at a temperature of about 700°C or higher and in the presence of an inert gas atmosphere.

Claim 12 (Currently Amended) An asymmetric field effect transistor (FET) comprising:

a patterned stack including at least a vertical semiconductor body having ~~exposed~~ sidewalls located on an upper non-recessed surface of an insulator that is located on a substrate;

a gate dielectric located on each ~~exposed~~ sidewall of said vertical semiconductor body;

a p-type gate portion located on one side of the vertical semiconductor body and an n-type portion located on an opposing side of the vertical semiconductor body, said gate portions forming an asymmetric FET that is ~~are~~ located on said upper surface of the insulator ~~substrate~~ and are separated from the vertical semiconductor body by said gate dielectric;

an interconnect located at least over said p-type gate portion and said n-type gate portion; and

a planarizing structure above said interconnect.

13. (Cancelled)

14. (Original) The asymmetric FET of Claim 12 wherein said p-type gate portion, said n-type gate portion and said planarizing structure are composed of a polySi-containing material or a semiconducting material.

15. (Original) The asymmetric FET structure of Claim 14 wherein said polySi-containing material comprises polySi or polySiGe.

16. (Original) The asymmetric FET of Claim 12 wherein said interconnect is highly resistant to dopant diffusion.

17. (Original) The asymmetric FET of Claim 12 wherein said interconnect is a conductive metal, metal silicide or metal nitride.

18. (Original) The asymmetric FET of Claim 12 wherein said planarizing structure is doped polysilicon.

19. (Cancelled)

20. (Original) The asymmetric FET of Claim 12 wherein said vertical semiconductor body has a hard mask present on an upper surface.

21. (Currently Amended) The asymmetric FET of Claim 20 wherein said hard mask is comprised of an oxide, nitride, ~~oynitride~~ oxynitride or multilayers thereof.

22. (Original) The asymmetric FET of Claim 12 wherein said n-type gate portion is comprised of N-doped polysilicon and said p-type gate portion is comprised of P-type polysilicon.

23. (Cancelled)

24. (Currently Amended) The asymmetric FET of Claim ~~23~~ 12 wherein said vertical semiconductor body and said substrate are components of a silicon-on-insulator material.

25. (Original) The asymmetric FET of Claim 12 wherein said planarizing material is a metal or metal alloy.

26. (Original) The asymmetric FET of Claim 12 further comprising source/drain regions in areas adjacent to the vertical semiconductor body.

27. (Original) The asymmetric FET of Claim 26 wherein said source/drain regions are doped so as to have either donor or acceptor impurities.

28. (Currently Amended) An asymmetric field effect transistor (FET) comprising:

a patterned stack including at least a vertical single crystal Si semiconductor body having ~~exposed~~ sidewalls located on an upper non-recessed surface of an insulator that is located on a substrate;

a gate dielectric located on each ~~exposed~~ sidewall of said vertical single crystal Si semiconductor body;

a p-type gate portion located on one side of the vertical single crystal Si semiconductor body and an n-type gate portion located on an opposing side of the vertical single crystal Si semiconductor body, said p-type and n-type gate portions are composed of polysilicon, and said gate portions forming an asymmetric FET that is ~~are~~ located on said upper surface of the insulator ~~substrate~~ and are separated from the vertical single crystal Si semiconductor body by said gate dielectric;

a metal silicide interconnect located at least over said p-type gate portion and said n-type gate portion; and

a planarizing doped polysilicon layer above said interconnect.